SUPPLEMENTAL EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

The following changes to the drawings have been approved by the examiner and agreed upon by applicant:

> On sheet 4 of the drawings, the lower drawing (currently captioned "4A", duplicating the caption of the upper drawing) is to be re-captioned "4B".

In order to avoid abandonment of the application, applicant must make these above agreed upon drawing changes.

REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance:

Claims 30-63 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention including a clear contact for the removal of charge carriers from an inner gate region that extends at least partially up to the clear contact, as recited in claim 30.

The closest prior art is NEESER ET AL: "DEPFET- a pixel device with integrated amplification" NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH, SECTION - A: ACCELERATORS, SPECTROMETERS, DETECTORS AND ASSOCIATED EQUIPMENT, NORTH-HOLLAND PUBLISHING COMPANY. AMSTERDAM, NL, vol. 477, no. 1-3, 21 January 2002 (2002-01-21), pages 129-136, XP004345526 ISSN: 0168-9002. It discloses a semiconductor structure comprising a weakly doped semiconductor substrate of a first (n) doping type, a highly doped drain region ("drain") of a second (p) doping type located at a first surface of the semiconductor substrate, a highly doped source region ("source") of the second (p) doping type located at the first surface of the semiconductor substrate, a channel ("p-channel") extending between the source region ("source") and the drain region ("drain"), a doped inner gate region ("internal gate") of the first (n) doping type, located in the semiconductor substrate, at least partially below the channel ("p-channel"), and a clear contact ("clear") for the removal of charge carriers from the inner gate region ("internal gate"). Note figures 1 and 2 of Neeser et al.

However, claim 1 further requires that the inner gate region extend at least partially up to the clear contact. Such a feature is not known from Neeser et al. (although it is shown in Applicants' figures 1a and 1b, where inner gate region IG extends up to, and overlaps, clear contact CL). The subject matter of claim 1 is therefore novel. The arrangement of the semiconductor structure of claim 1 makes it possible to clear the signal electrons that have accumulated in the inner gate region IG by means of a low electrical voltage, with the result

that the power and efficiency of the semiconductor structure are improved. Therefore, Neeser et al. neither discloses nor suggests the subject matter of claim 1.

2. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

- ***Conclusion***

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Sue A. Purvis, at 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-

direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thomas L Dickey/

Primary Examiner, Art Unit 2826